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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/405,618	09/24/1999	JAMES S. BLOMGREN	31876.0140	9689

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EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

FN

Office Action Summary	Application No. 09/405,618	Applicant(s) BLOMGREN ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10-16-02* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3, 6-8, 11-13, 16-18 and 21-23* is/are pending in the application.

4a) Of the above claim(s) *4,5,9,10,14,15,19,20,24 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 6-8, 11-13 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 October 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 6
4) ☒ Interview Summary (PTO-413) Paper No(s). 8 .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Amended claims 1-3, 6-8, 11-13, and 16-18 have been presented for reconsideration in light of Applicant's amended specification. Claims 1-3, 6-8, 11-13, and 16-18 have been reconsidered and rejected. Claims 4, 5, 9, 10, 14, 15, 19 and 20 have been excluded from consideration as per Applicant's request. Claims 24 and 25 have been canceled, without prejudice, as per Applicant's request, *see page 12 of Applicant's amendments.*

Response to Arguments

2. Applicants arguments filed on 16 & 18 October 2002 have been fully considered. Examiners response is as follows:

Regarding applicants submission of amended drawings; The amended drawings filed on 18 October 2002 have been reviewed by the examiner, figure1 is approved by the examiner.

Regarding applicants submission of the amended Table on page 5 of Applicant's Specification; The amended specification as regards the changes to page 5 of Applicant's specification have been approved by the Examiner.

Regarding applicants response to objection to improper incorporation; The applicant has amended page 4 of the specification with the serial number and Patent number of the Applicants co-pending U.S. Patent application, which has now issued as a U.S. Patent and as such the Applicant has fulfilled the requirement as the guidelines discloses;

Guidelines for situations where applicant is permitted to fill in a number for Application No. _____ left blank in the application as filed can be found in In re Fouche, 439 F.2d 1237, 169 USPQ 429 (CCPA 1971).

It is noted by the Examiner that the Applicant has disclosed that this is a U.S. Patent Application and has also included the U.S. Patent number of the issued U.S. Patent and has removed any ambiguity as to the unique identity of the document for incorporation by reference.

Regarding Applicant's response to Examiners Claim Rejections Under 35 USC 102(b);

Applicants have argued that the Giramma (U.S. Patent Number 5,706,476) reference as follows;

> Giramma discloses a methodology by which a binary-based logic design can be simulated using a combination of an 8-state simulation model and a 4-state simulation model. Giramma's 8-state model is a modification of the standard, well-known MVL-9 model discussed in the instant application and in the IEEE Specification Std-logic-11 164, and his 4-state model is a modification of the well-known prior art 4state model discussed in the instant application. Like the discussion in the current application at page 5, line 14 through page 6, line 20, Giramma discusses the impracticality of using extended-state models, such as an 8- or 9-state simulation model, to simulate complex binary gates, because the size of the truth-tables involved cannot be accommodated in the memory of a standard computer simulation workstation. The present application discloses that designers attempting to employ extended-state simulations for complex binary logic have developed workaround solutions, such as mapping large truth table functions to multiple smaller truth table functions, or ignoring certain states within a multiple state model for certain designs. Application at p. 6, lines 16-20.

Applicants are arguing that the Giramma and IEEE references do not teach an "N-NARY" signal model, the Examiner respectfully transverses Applicant's argument and states that an "N-NARY" signal model can be a "Binary" signal model if one sets the "N" in "N-Nary" to the value of 2. In the Applicant's amended Claims the term non-binary is inserted and therefore excludes a binary signal model, the Examiner asserts that the signal model disclosed in the Giramma and the IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164), can model an "N-Nary" non-binary logic signal, note that in the IEEE reference is disclosed as having 8 different states, *(see page 15, Annex A)*. Therefore the IEEE reference discloses an "N-NARY" signal model where "N" is greater than 2, by Applicant's own admission the Giramma reference discloses a "4" state model and therefore "N" is greater than 2

and is therefore a valid "N-NARY" signal model as is claimed in applicants amended claims. Although the applicant has clarified that, "The present invention is thus an entirely new method and apparatus that enables designers to simulate nonbinary logic, such as N-NARY logic", the Examiner asserts that the amended claim language does not clearly disclose this "new" method in such a manner as to distinguish the Applicant's invention from the Giramma and IEEE references.

The Applicant further states;

Part of the Examiner's confusion is undoubtedly related to terminology. Treatises that discuss prior art multiple-state simulation models for binary logic (including the IEEE standard and including Giramma) often use the phrases "logic state," "logic value", and "decimal value" somewhat interchangeably. For example, Giramma describes the various states in an extended-state simulation abstraction as "strengths or values" at col. 1, lines 39, 42, and 47, and describes the various states in his 8-state abstraction as having "decimal values" in Table 2. However, in Applicant's lexicon as applied to a binary signal, the phrases "logic value" and "decimal value" refer only to the true-or false, high-or-low, 1-of-0 nature of the signal-the information used to determine whether a binary signal is asserted or not. In Applicant's lexicon, a signal's "logic value" or "decimal value" bears no relation to its drive state or whether the signal has a status other than asserted or not asserted (i.e., whether a signal is undefined, uninitialized, or high-impedance). In the present invention, a signal model is a representation of a signal that is in a state that includes its logic value, its signal strength, and its signal status-all three of which are separate pieces of information about the signal. Using Applicant's lexicon, then, every prior art simulation model used for binary logic, whether it employs the simplest 2-state logic model or the most complex extended-state model, can only simulate signals that have a "decimal value" or "logic value" of 1 or 0, regardless of the terminology used that may confuse a signal's "logic value" or "decimal value" with the number of states that the model can represent. In the more sophisticated models, as described in the instant application and in Giramma, these binary signals having a decimal value or logic value of either 1 or 0 also have a "drive state," which may be either strongly driven (typically denote as S) or weakly- driven (typically denoted as R). Notably, a strongly-driven high-voltage binary signal does not have a different signal value, decimal value, or logic value than a weakly driven high-voltage binary signal; both signals are asserted and have a logic value of 1. They simply have different drive strengths. Similarly, like a signal's drive strength, prior art simulation models can simulate other characteristics of signals that are not the same as the signal's logic value-for instance, a signal with unknown or indeterminate value (X), a high-impedance signal (Z), an uninitialized signal (U), or an undefined signal (D). These kinds of signals have no logic value-they are unknown, high-impedance, uninitialized, or undefined. These are not "logic values," they are signal characteristics that can be meaningfully simulated.

The imprecision regarding the prior use of the phrases "logic value", "signal value" and "decimal value," to describe a modeled signal having a certain signal state that may include a logic value, a drive strength, and a signal status has led to the use of the terms "multivalue logic" and "multiple value logic" to describe models that include extended-state model abstractions, even though these extended-state models are used to simulate binary logic, which is not multivalue logic. Applicant's use of the terms "multiple value logic" or "multivalue logic means nonbinary logic, i.e., N-NARY logic. In the present invention, and using Applicant's precise terminology, a 1-of-N N-NARY signal's "logic value" or "decimal value" means the value encoded in the signal's multiwire bundle, as indicated by which one of the wires within the signal bundle is asserted. See Table 2, page 7. Therefore, in the present invention, an N-NARY signal model can have more than two logic values-indeed, virtually every signal in the NNARY logic family has more than two logic values. The signal illustrated in Table 2 has four logic values or decimal values-this signal can have a logic value or decimal value of 0, 1, 2, or 3. In the present invention, a signal having one of these logic values may also have a certain drive strength-it may be strongly driven, moderately driven, or weakly driven-*but an N-NARY signal's drive strength does not change its logic value.* As in the prior art methodologies, and using Applicant's definition a signal's logic value, drive strength (strong or resistive) is simply a description of a signal characteristic that is not the same as the signal's logic value.

Using Applicant's lexicon, then, neither Giramma nor the IEEE specification disclose the simulation of multivalue signals-they simply disclose the simulation of binary signals, wherein the signal model is capable of simulating the binary signal's logic value-0 or 1-plus a number of characteristics that includes the drive strength of the logic value, or the fact that a binary signal has no logic value or drive strength at all, but rather, is undefined, uninitialized, or high-impedance. While the IEEE reference refers to the undefined, unitialized, and high-impedance signal states as "logic values," in Applicant's parlance, these are more properly considered to be signal characteristics. In Applicant's parlance, a 1-of-N signal's logic value is an integer that carries meaningful encoded information rather than signal status information such as undefined, unitialized, or high-impedance.

Given this clarification of terminology, the difference between the IEEE specification binary-based methodologies, or Giramma's methodology (which is simply a modification and combination of the IEEE methods), and the present invention is clear. The IEEE models and Giramma's method are applicable only to binary logic, and simulate only binary signals and their various characteristics of interest to binary logic designers.

Applicant's states that in the Giramma's reference that, in Applicant's lexicon, a signal's "logic value" or "decimal value" bears no relation to its drive state or whether the signal has a status other than asserted or not asserted" the Examiner asserts that a Logic state of "1" does describe a drive state and that a logic state of "0" describes another drive state. In positive logic a Logic state of "1" denotes that the previous logic gate is operating in a "Cut-off" drive state, that

gate is "turned off" or not conducting what so ever, when that same logic gate is in a "0" state that gate is in a drive state of fully conducting either in saturation, as in pre- Schottky TTL digital electronics or just at "turn on" as in (Low Power Schottky) LS-TTL circuits that are not deep into saturation, in the modern IC where high speed CMOS logic gates are utilized the same conditions are true. Applicant further states, "Applicant's use of the terms "multiple value logic" or "multivalue logic means nonbinary logic, i.e., N-NARY logic. In the present invention, and using Applicant's precise terminology, a 1-of-N N-NARY signal's "logic value" or "decimal value" means the value encoded in the signal's multiwire bundle, as indicated by which one of the wires within the signal bundle is asserted." The Examiner asserts that there is nothing in the Applicant's amended claims to clearly distinguish the differences between what Applicant states to mean "multi value logic" and the term as it is used in the Giramma reference and the IEEE reference, therefore the Examiner asserts that these references do directly apply to a nonbinary N-NARY logic signal because both references disclose a signal model wherein there are more than "2" binary states that are being modeled. Therefore Examiner asserts that the, "confusion is undoubtedly related to terminology" is reflected in the Applicant's amended claims and as such the Examiner maintains the 35 U.S.C. 102 (b) rejections.

The Applicant further states; "for instance, a signal with unknown or indeterminate value (X), a high-impedance signal (Z), an uninitialized signal (U), or an undefined signal (D). These kinds of signals have no logic value-they are unknown, high-impedance, uninitialized, or undefined. These are not "logic values," they are signal characteristics that can be meaningfully simulated." The Examiner asserts, that a high-impedance signal (Z) does have a Logic value in that the simulated design in a Hardware Description Language, such as VHDL, will treat the (Z)

value in its logic determination differently from a non-high impedance state. For example, in the simulation of a BUS (i.e. multiwire bundle) of signals, two sets of gates are sharing the same group on connections to an array of memory elements (flip-flops). If one set of the gates is declared to be "tri-stated" or in a "Z" state the simulation knows to ignore any fan-out requirements of that array of gates and not to factor in the logic state of those gates in making any determination as to the final logic signal of that array of flip-flops. Therefore the Examiner asserts that these kinds of signals have a very significant logic value that must be taken into account when operating a logic simulation.

The Applicant further argues; The present invention models nonbinary signals—signals capable of having meaningful logic values, independent of drive strength or other signal characteristics, that are something other than 0 or 1. The Examiner asserts that the Applicant is still representing logic states, the Applicant is just representing the logic states in groups and therefore representing how many of the different signals on the bundle are asserting a logic "1" vs. a logic "0", this methodology is disclosed in the IEEE Standard Multivalue Logic System for VHDL Model Interoperability, see TYPE std_logic_vector is ARRAY (NATURAL RANGE <>) Of std_logic; Page 2 of IEEE spec. Therefore the Examiner respectfully disagrees with Applicant's arguments and upholds his U.S.C. 102(b) rejection based on Applicant's amended claims.

Applicant argues;

First, as discussed above, Applicant's use of the term "decimal value" or "logic value" means the logic value of the signal. In a binary signal, that logic value can only be 0 or 1, regardless of the drive state or other signal characteristics. In nonbinary N-NARY logic, 1-of-N signals can have N logic values, typically described as integers from 0 to (N-1). See Table 2. Consequently, neither Giramma nor the IEEE specification teach modeling a 1-of-N logic signal having a logic value that ranges from greater than 1 or equal to or less than 31. Giramma's 32-bit

"zoom" words have nothing to do with the logic value of a modeled signal; they are simply a convenient methodology to access the truth tables Giramma uses to determine a gate's output and send "directives" (i.e., inputs and state abstractions) to the next downstream gate. As the present invention is used in a simulation that does not utilize truth tables, Giramma's 32-bit "zoom" words are wholly unrelated to any feature or function of the present invention.

The Examiner asserts that in fact the "zoom" words as described in the Giramma reference read exactly on the Applicant's technology by abstracting the states of multiple logic gates in a "wire" bundle along with other signal attributes such as drive strength is precisely what Giramma is describing with the zoom words.

As stated in Giramma ***(Col. 4 Lines 59-63);*** "mapping the high-impedance state of the eight-state abstraction into the undefined state of the four-state abstraction, as is described above by the use of zoom words..." Here the reference specifically describes mapping different characteristics of a "Bundle" of logic signals into one "zoom" word, which describes precisely what applicant is disclosing in the amended claims. Stating that the Giramma reference doesn't read on the applicant's technology because the "zoom" words are used to access a look up table ignores the essence of applicants invention which is to abstract several signal wires into one 32 bit word and represent an "N-Nary" set of modeled logic signals, this is exactly what the Giramma reference is doing with the "zoom" words.

Applicant further argues;

Similarly, Giramma's assignment of a "decimal value" to each modeled state (See Table 2, col. 6) is completely arbitrary, the "decimal value" is only a pointer that cross-references to a specific modeled state and does not relate to the actual logic value (0 or 1) or drive state (S or R) or other signal characteristic (U, Z, or X) capable of being modeled. In contrast, the signal value in the claimed signal model is the exact logic value or decimal value of the 1-of-N signal being modeled. The signal value of the model must be identical to the decimal value or logic value of the signal being modeled or the simulation will not run correctly.

The Examiner asserts that cross-referencing to a modeled state is what Applicants invention is doing by representing the signal strengths and the signal characteristics as well as the logic states in a 32 bit word. The Examiner further asserts that there is nothing in Applicants amended claims that shows what the specific format or level of abstraction is that Applicant requires for Applicant's invention and therefore the Examiner maintains that the Giramma's "zoom" word does read directly on Applicants amended claims and therefore upholds the 35 U.S.C. 102(b) rejection.

Nonstatutory Double Patenting

A rejection based on nonstatutory double patenting is based on a judicially created doctrine grounded in public policy so as to prevent the unjustified or improper timewise extension of the right to exclude granted by a patent. In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); In re White, 405 F.2d 904, 160 USPQ 417 (CCPA 1969); In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968); In re Sarett, 327 F.2d 1005, 140 USPQ 474 (CCPA 1964).

3. **Claims 1-3, 6-8, 11-13, 16-18 and 21-23** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claims 1-7, 8-14, 15-21, 22-28 and 29-35** in view of **Leight et al. U.S. Patent 6,289,497.**

Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing a signal naming convention that describes an N-nary logic circuit.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have used the system as described in the *Leight et al.* reference to model signals in an N-nary logic simulation because, (...the tool of the present invention does not require a semiconductor designer to develop a schematic and a separate behavioral model that must be verified against each other. Instead, the design tool of the present invention separately compiles both a behavioral model and a physical circuit description from one syntax statement. The present invention guarantees that the schematic and the behavioral model will "match up," greatly reducing the man-hours needed to design semiconductor circuits, *Leight et al. Col. 2 Lines 49-57*)

Specifically the *Leight et al.* reference discloses as signal model for N-nary logic simulation ***Leight, Claim 6,*** wherein there is a signal strength field, ***Claim 2, a signal degree field,*** and a signal definition field ***Claim 4, a mux select expression, an arithmetic expression, a logical expression, a multiple output expression, a capacitance isolation expression, or a shared node expression.***

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-3, 6-8, 11-13, 16-18 and 21-23 are being rejected under 35 U.S.C. 102(b) as being clearly anticipated by Giramma "METHOD AND APPARATUS FOR USE OF THE UNDEFINED LOGIC STATE AND MIXED MULTIPLE-STATE ABSTRACTIONS IN DIGITAL LOGIC SIMULATION" U.S. Patent 5,706,476.** *Giramma* discloses, Taking as per claim(s) 1, 6, 11, 16 and 21 for example: A model that simulates logic signals capable of having more than two unique values and one or more unique drive states. **Col. 1, lines 20-63** and in claim 1 *Giramma* recites, "A computer-assisted logic gate simulation method for simulating a circuit that includes plural logic gates characterized by differing output state abstractions, " whereby the unique driver states comprise: a signal value field *Giramma* discloses, "Those of skill in the art will appreciate that by directive production is meant any technique for signaling or otherwise communicating to a downstream connected primitive the possible next-state of its inputs based upon a transition of state of an output of an upstream primitive." **Col. 5, Lines 13-18**. *Giramma* recites a signal strength field, "In addition to these state abstractions, some logic simulators use a 3-state model coupled with essentially unlimited strengths or values." **Col. 1, Lines 51-53.** *Giramma* also teaches a signal definition field which comprises information that conveys whether the signal being modeled holds a defined value or an undefined value, "Also preferably, the 4-state abstraction includes an undefined state such as undefined state XS described above." **Col. 4, Lines 53-55.**

With respect to claims 2,7,12,17 and 22 *Giramma* discloses, "Those skilled in the art will appreciate that 32-bit `zoom` words, in accordance with the preferred embodiment of the invention, are used to obtain indices into various tables for next-state logic evaluations." **Col. 6, Lines 51-54.**

With respect to claims 3, 8, 13, 18 and 23 *Giramma* discloses, "Multiple-Value Logic 9-state model (MVL-9) of 0, 1, X at strong and resistive strengths or values, as well as high-impedance uninitialized, and undefined (0S,1S,XS,0R,1R,XR,Z,U,D). " **Col. 1, Lines 46-49.**

5. **Claims 1-3, 6-8, 11-13, 16-18 and 21-23 are being rejected under 35 U.S.C. 102(b) as being clearly anticipated by the IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164).** *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* discloses, with respect to claim(s) 1, 6, 11, 16 and 21, logic signals capable of having more than two unique values and one or more unique drive states. On **Page 2,** *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* recites, SUBTYPE UX01Z IS resolved std_ulogic RANGE 'U' TO 'Z'; -- ('U','X','0','1','Z'). *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* recites on in **Annex A on Page 15**, "A.1 Value system...one must interpret the meaning of each of the elements as provided by the standard. Type std_ulogic is ('U', Uninitialized state Used as a default value 'X', Forcing Unknown Bus contentions, error conditions, etc. '0', Forcing Zero Transistor driven to GND '1', Forcing One Transistor driven to VCC 'Z', High Impedance 3-state buffer outputs 'W', Weak Unknown Bus terminators 'L', Weak Zero Pull down resistors 'H', Weak One Pull up resistors '-' Don't Care Used for synthesis and advanced modeling); " which is a signal value field in the Multivalue Logic System as well as a signal definition field. *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* teaches on **Page 15, Annex A;** " Therefore, a number of strength stripper functions have been designed to transform 'Z', 'W', 'L', 'H', and '-' into their corresponding forcing strength counterparts." This teaches a signal strength field.

With respect to claims 2, 3, 7, 8, 12, 13, 17, 18, 22 and 23 *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* teaches on **Page 15, Annex A,** "Forcing Zero Transistor driven to GND, Forcing One Transistor driven to VCC, Weak Zero Pull Down resistors, Weak One Pull up Resistors.

6. **Claims 1-3, 6-8, 11-13, 16-18 and 21-23 are being rejected under 35 U.S.C. 102(b) as being clearly anticipated by "On the Use of VHDL as a Multi-Valued Logic Simulator" by C. Rozon, IEEE 1996** hereafter referred to as the **Rozon** reference.

As regards **Claims 1, 6, 11, 16 and 21,** the *Rozen* reference teaches a signal model for an N-Nary logic simulation **Pages 110-115.** wherein the logic value comprises an integer greater than 1 **Table 1, page 110**, and a signal strength **Table 1, page 110** and signal definition **Page 112, and Table 2**.

As regards **Claims 2, 7, 12, 17 and 22** the *Rozon* reference discloses an integer less than or equal to 31 **ANNEX 1, page 114.**

As regards **Claims 3, 8, 13, 18 and 23** the *Rozon* reference discloses the signal strength being high-impedance, weakly-driven, moderately driven or strongly-driven, **Page 110 Table 1.**

Conclusion

7. The Examiner concludes that the Applicants arguments are unpersuasive and that the Examiners old and new rejections be upheld. Claims 6, 7 and 8 are renumbered 4, 5, and 6, Claims 11, 12, and 13 are renumbered 7, 8, and 9, Claims 16, 17 and 18 are renumbered 10, 11, and 12, Claims 21, 22 and 23 are renumbered 13, 14 and 15.

THIS ACTION IS MADE FINAL, in response to amendment. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100